IN THE SPECIFICATION:

Please insert the following new paragraph after the Title and before the "Technical Field":

-- Related Application

This application is the U.S. National Phase under 35 U.S.C. § 371 of International Application No. PCT/JP2004/009811, filed on July 9, 2004, which in turn claims the benefit of Japanese Application No. 2003-339030, filed on September 30, 2003, and Japanese Application No. 2003-362216, filed on October 22, 2003, the disclosures of which Applications are incorporated by reference herein. –

Please amend the paragraph beginning on page 25 at line 13 and bridging page 26 as follows:

Integrated circuit device 26# in accordance with Embodiment 4 of the present invention differs from integrated circuit device 26a shown in Fig. 15 in that reconfigurable circuit 12 is replaced by reconfigurable circuit 12#a and that setting portion 14 is replaced by setting portion 14#. Except for this point, the device is the same, and therefore, detailed description thereof will not be repeated. Reconfigurable circuit 12#a has a so-called pipeline configuration, and by changing setting, functions can be changed. Setting portion 14# has a first circuit setting portion 15a, a second circuit setting portion 15b, a third circuit setting portion 15c and a circuit process control portion 16#, and supplies setting data 40 for forming an intended circuit in reconfigurable circuit 12#a. Circuit process control portion 16# supplies outputs from the first to third circuit setting portions 15a to 15c to reconfigurable units, which will be described later, forming stages of the pipeline of reconfigurable circuit 12#a, in a prescribed order. Further, the first to third circuit setting portions 15a to 15c are respectively provided corresponding to the reconfigurable units, which will be described later. Setting portions 14 and 14# may be formed by a memory storing setting data and the like and a so-called program counter designating a memory address, that is, an address of the memory.

Please amend the paragraph beginning on page 28 at line 24 and bridging page 29 as follows:

Referring to Fig. 30, in the first step cycle (1st step cycle), divided unit FA1 is mapped to the first stage, and the input signal IP is input. A logic operation is executed in divided unit FA1, and thereafter, the result of logic operation is held by the connecting portion + FF circuit 52#a described above. In the next step cycle (2nd step cycle), divided unit FA2 is mapped to the second stage, and divided unit FB1 receiving the input signal QP is mapped to the first stage. Accordingly, in the first stage, the logic operation of divided unit FB1 is executed, and the result of logic operation is held by the connecting portion + FF circuit 52 described above. In the second stage, receiving the input of the result of logic operation that has been held by the preceding stage, divided unit FA2 executes a prescribed logic operation, and the result of logic operation is held by the connecting portion + FF circuit 52. In the next step cycle (3rd step cycle), divided unit FA3 is mapped to the third stage, divided unit FB2 is mapped to the second stage, and divided unit FC1 receiving input signal MIP(-1) and input signal MQP(-1) is mapped to the first stage. Accordingly, in the third stage, a logic operation of divided unit FC1 is executed, and the result is output from reconfigurable circuit 12#a. The output result is held by internal state holding circuit 20, and transmitted to the input side of reconfigurable circuit 12#a through path portion 24. Specifically, the signal transmitted to switching circuit 28 through path portion 24 is input to reconfigurable circuit 12#a in response to an instruction from circuit processing control portion 16#. In the next step cycle (4th step cycle), divided unit FA4 is mapped to the first stage, divided unit FC2 is mapped to the second stage, and divided unit FB3 is mapped to the third stage. Thereafter, in the similar manner, divided units FA1 to FA6, FB1 to FB6 and FC1 to FC6 are mapped successively in order, to the ALUs of the first to third stages of reconfigurable circuit 12#a, in accordance with the flow of signal processing of respective circuits FA to FC.